REMARKS/ARGUMENTS

In light of the above amendments and remarks to follow, reconsideration and allowance of this application are respectfully requested.

Claims 1-55 are pending in this application.

A terminal disclaimer is submitted to overcome the double patenting rejections.

Claims 1-55 have been amended to overcome the rejections under 35 U.S.C. § 101 and 35 U.S.C. § 112, second paragraph.

Claims 10 and 12-16 were rejected under 35 U.S.C. § 102 as being anticipated by EP 0459931 ("*Bahr*"). Further, claims 1-4, 8-9, 27-30, 34-38 and 41-42 were rejected under 35 U.S.C. § 103(a) as being obvious over *Bahr* in view of U.S. Patent No. 5,506,987 ("*Abramson*"); claims 11 and 21-25 were rejected under 35 U.S.C. § 103(a) as being obvious over *Bahr*; claims 17-20, 26, 43-50 and 53-55 were rejected under 35 U.S.C. § 103(a) as being obvious over *Bahr* in view of U.S. Patent No. 5,452,452 ("*Gaetner*"); and claims 5-7, 31-33, 39-40 and 51 were rejected under 35 U.S.C. § 103(a) as being obvious over *Bahr* in view of *Abramson* and *Gaetner*.

The present claims are directed to executing processor tasks on a multiple processor system. Each of independent claims 1, 10, 21, 26, 27 and 43 includes the requirement of "migrating" a processor task from one processing unit to another processing unit in accordance with the priority of the processor tasks.

The Examiner admitted that *Bahr* does not teach "migrating" processor tasks from one processing unit to another processing unit based on the priority levels of the tasks, as claimed. Contrary to the Examiner's statements, *Abramson* or

Gaetner do not cure the deficiencies of *Bahr*. Although *Abramson* describes migrating of processor tasks, *Abramson* teaches migrating processing tasks for balancing system processing work load among processors. (*See Abramson*, Col. 2, ln. 40-53 and Col. 6, ln. 36-41). In addition, in contrast to the Examiner's statement, *Gaetner* does not describe migrating processor tasks from one processor to another. Instead, *Gaetner* teaches that a first processor already running a high priority task causes a second processor to handle a priority processing task, where the second processor's processing of another task is interrupted (preempted), as needed. According to *Gaetner*:

> … [A] processor running a high priority process … cause[s] a processor running a lower priority to handle the interrupt. ….
>
> If it is imperative that an interrupt be handled immediately, the current processor can cause another processor to be preempted by sending that processor a signal …. The signaled processor, 5 process is preempted when it receives the signal. The process running on the signaled processor can then determine whether it will handle the interrupt ….

(*See Gaetne*r col. 7, ln. 56 - col. 8, ln. 5)

Accordingly, *Bahr* does not anticipate the present invention, and *Bahr*, *Abramson* and *Gaetner*, alone or in combination, fail to obviate the present invention, such that the rejected claims should now be allowed.

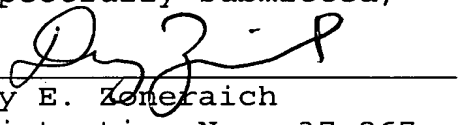
In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he/she telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095.

Dated: April 16, 2008

Respectfully submitted,

By 

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